Atomic Layer Deposition Assisted Pattern Multiplication of Block Copolymer Lithography for 5 nm Scale Nanopatterning

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5-nm-scale line and hole patterning is demonstrated by synergistic integration of block copolymer (BCP) lithography with atomic layer deposition (ALD). While directed self-assembly of BCPs generates highly ordered line array or hexagonal dot array with the pattern periodicity of 28 nm and the minimum feature size of 14 nm, pattern density multiplication employing ALD successfully reduces the pattern periodicity down to 14 nm and minimum feature size down to 5 nm. Self-limiting ALD process enable the low temperature, conformal deposition of 5 nm thick spacer layer directly at the surface of organic BCP patterns. This ALD assisted pattern multiplication addresses the intrinsic thermodynamic limitations of low χ BCPs for sub-10-nm scale downscaling. Moreover, this approach offers a general strategy for scalable ultrafine nanopatterning without burden for multiple overlay control and high cost lithographic tools.

1. Introduction

Directed self-assembly (DSA) offers the device-oriented nanopatterns based on BCP self-assembly and has triggered enormous attentions for semiconductor lithographic applications.[1–10] To date, various BCPs with different chemical compositions are explored for DSA process.[11–37] Among them, low χ BCPs, such as polystyrene-block-poly(methyl methacrylate) (PS-*b*-PMMA), has been extensively employed due to several advantages. Well-established surface neutralization method readily attains the vertical lamellar or cylinder nanostructures with high aspect ratio via fab-friendly temperature annealing process.[1–7,9,12,15–17,19,24–29,32,33] Selective etching of PMMA nanodomains provides vertical side wall profile of nanotemplates, which is greatly beneficial for subsequent pattern transfer.[19,22,23,33,35] Nevertheless, the low χ characteristic of PS-*b*-PMMA inherently limits the minimum feature size around 12 nm,[30,34] which is a significant bottleneck for the continuous downscaling requirements for sub-10-nm scale pattern in semiconductor industry.

ALD is a specific modification of chemical vapor deposition for atomic scale film thickness controllability.[37–41] In an ALD process, intermediate purging steps completely remove the excess precursors and reaction byproducts prior to the introduction of the next deposition layer. Cyclic repetition of such alternative steps enables unprecedented self-limiting atomic scale film growth with large-area uniformity and conformability. Besides, ALD is compatible to a low deposition temperature, which is highly desired for temperature sensitive organic or polymeric substrates.[24,25,36–38,41–44] Owing to those advantages, ALD is considered a reliable technology to satisfy the stringent requirement for next generation semiconductor processing.

In this work, we introduce an efficient and robust pattern density enhancement method for ultrafine BCP self-assembled nanopatterns enabled by ALD. Pattern multiplication methods, such as double patterning, have been employed in semiconductor industry in conjunction with conventional photolithography, such as ArF lithography.[45–49] Meanwhile, due to the ultrafine feature size and relatively low aspect ratio of BCP self-assembled nanostructures, it is unclear whether such a pattern density principle is compatible to BCP nanopatterning. We address this challenge and successfully demonstrate the nanopatterns with minimum feature size down to 5 nm. Notably, this pattern multiplication employing ALD process is scalable to large area and utilizes self-alignment strategy that multiple overlay control is spontaneous.

2. Results and Discussion

Our pattern density enhancement process for BCP nanopatterning is schematically described in **Figure 1**. First, silicon

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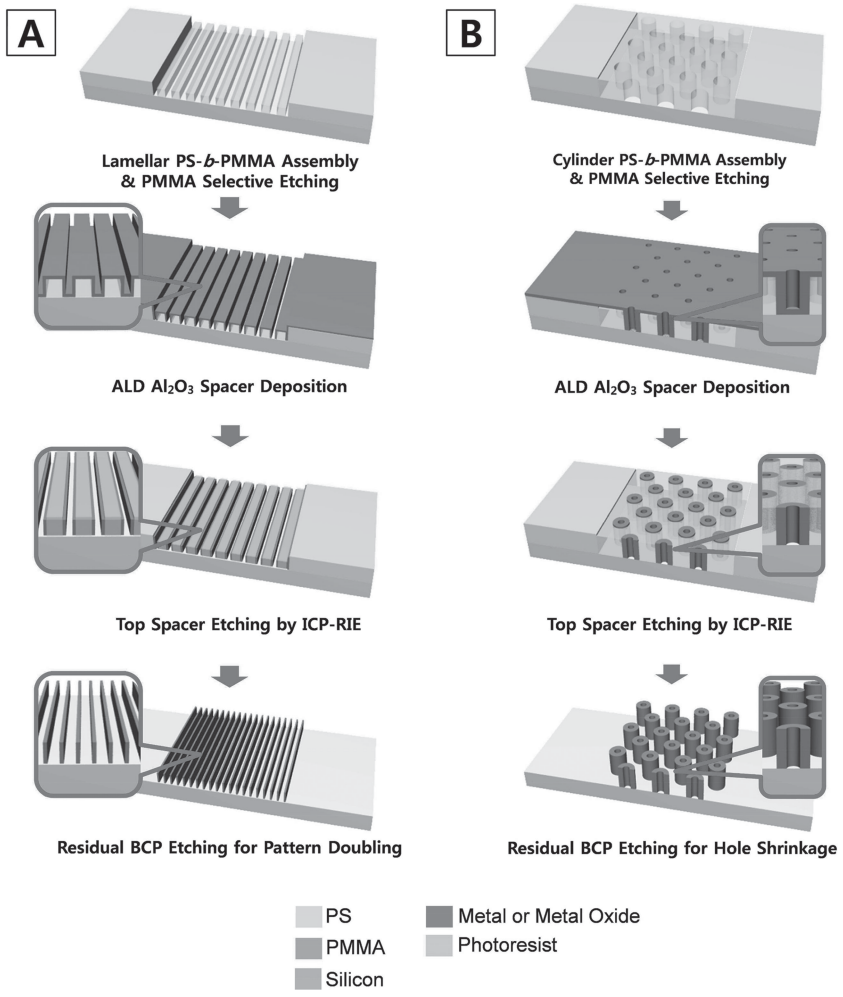

Figure 1. Schematic procedure for ALD-assisted pattern multiplication of directed block copolymer self-assembly with a) lamellar block copolymers and b) hexagonal cylinder block copolymers.

substrates are neutrally modified with poly(styrene-ran-methyl methacrylate) (P(S-*r*-MMA)) random copolymer brush treatment. This surface modification balances the interfacial tensions of PS and PMMA components to bottom substrate to yield surface perpendicular lamellar or cylinder nanodomains in PS-*b*-PMMA thin films as equilibrium morphology. A negative tone photoresist (SU8) was spin cast on the substrate and topographically patterned by I-line photolithography (wavelength: 365 nm and intensity: 9.5 mW cm^{-2}). PS-*b*-PMMA thin films were spin-casted within the topographic trenches of the photoresist patterns and thermally annealed at 280 °C to yield highly ordered equilibrium morphology. Unlike positive tone photoresists with thermoplasticity, crosslinked SU8 pattern maintained the pattern integrity during the high temperature annealing. The thickness of BCP thin films was approximately controlled around 100 nm, while photoresist pattern height was maintained at 150 nm. Figure 1A schematically illustrates highly aligned lamellar array formation of symmetric BCP thin film within parallel photoresist trenches. Asymmetric BCPs may form hexagonal vertical cylinder array after the same experimental procedure, as illustrated in Figure 1B. The PMMA nanodomains in PS-*b*-PMMA thin films were selectively removed by wet etching (acetic acid washing after UV treatment) or dry etching (O_2 reactive ion etching (RIE)) process. Dry etching is desired particularly for lamellar nanopatterns to avoid pattern collapse, which is readily caused by the capillarity effect from wet chemicals. Fortunately, PS and PMMA show sufficiently high etching contrast to conventional O_2 RIE process. By contrast, wet etching can effectively remove PMMA cylinder nanodomains enclosed by PS matrix without concerning pattern collapse or etching selectivity.

After selective etching of PMMA nanodomains, nanoscale thick inorganic spacer layers were deposited by ALD at the surface of remaining topographic PS patterns. Our approach employing ALD facilitates conformal and low temperature deposition of various oxide films at nonplanar polymer surfaces. This versatility was confirmed by the control tests for Al_2O_3, TiO_2, and ZnO performed at various temperatures (150 °C, 180 °C, 200 °C, 220 °C, and 250 °C) (Supporting Information, Figure S1). Trimethylaluminum (TMA; $Al(CH_3)_3$),[24,25,38,41,50,51] titanium isopropoxide (TTIP; $Ti(OC_3H_7)_4$),[43,52–56] and diethylzinc (DEZ; $Zn(C_2H_5)_2$)[57–59] were used as Al, Ti and Zn metal precursors, respectively. The metal precursors equilibrated at predetermined temperatures (TMA: 10 °C, TTIP: 50 °C, and DEZ: 10 °C) and H_2O were alternately entrained in the N_2 carrier flow using gas switching valves. N_2 carrier gas pressure was 1.0 Torr. The transient increase of precursor gas pressure upto 0.1 Torr were monitored, while the reactants were repeatedly introduced into the N_2 carrier flow. The upper temperature limit for conformal film deposition was found around 150 °C, above which the UV radiated PS nanotemplates were noticeably degraded.

In this work, Al_2O_3 was chosen as spacer layer materials for pattern density multiplication. Al_2O_3 is one of the most widely investigated materials for ALD process.[24,25,38,41,50,51] High quality Al_2O_3 films are attainable by ALD with a variety of available precursors and relatively short cycle times.[24,25,41] We investigate the influence from the deposition temperature on the qualities of Al_2O_3 films from 130 to 150 °C. A unit ALD cycle consisted of TMA vapor pulse with 50 sccm N_2 carrier gas, purge pulse with 50 sccm N_2, H_2O vapor pulse with 50 sccm N_2 carrier gas, and the second 50 sccm N_2 purge pulse. The time for one complete ALD cycle ranged from 20.4 s at 150 °C to 30.4 s at 130 °C. A long purge time was required at a low deposition temperature to avoid the multiple layer deposition caused by insufficient purge times. Typically, conformal deposition of Al_2O_3 spacer layer on BCP was performed at 130 °C (Supporting Information, Figure S2), where the growth rate of Al_2O_3 film was 1.67 Å/cycle. The optimal spacer layer thickness

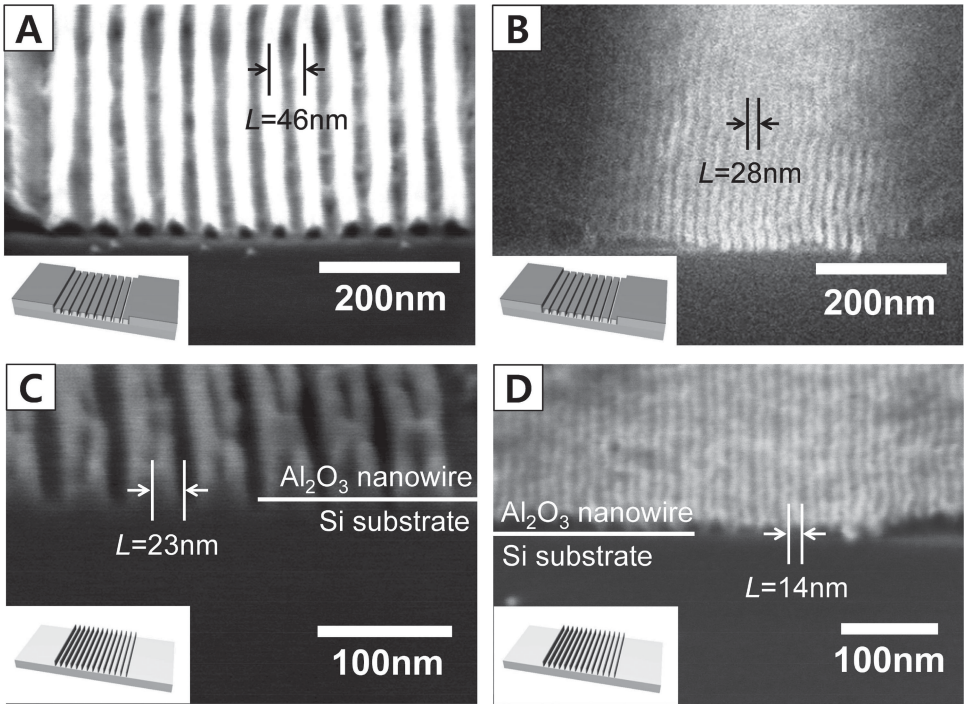

Figure 2. SEM images of Al_2O_3 coated BCP lamellar nanopatterns and pattern density doubled Al_2O_3 nanopatterns. Conformal Al_2O_3 layer coated PS nanotemplates made from PS-*b*-PMMA copolymers with a) M_n = 94 kg mol^{-1} and L = 46 nm and b) M_n = 50 kg mol^{-1} and L = 28 nm. Al_2O_3 nanopatterns with pattern periods of c) L = 23 nm and d) L = 14 nm.

was found to be 5 nm for robust pattern multiplication without pattern collapse. According to the 2012 ITRS roadmap, the critical dimension (CD) for spacer layer thickness in pattern density multiplication requires overlay control between 1.8 and 5.7 nm, when the half pitches of DRAM were 8.9 and 28.0 nm, respectively.[48] Our low temperature Al_2O_3 ALD sufficiently fulfills this stringent requirement.

After spacer layer formation, the top surface of spacer layer was etched by inductively coupled plasma reactive ion etching (ICP-RIE). We note that conventional RIE is unsuitable for the precise etching of 5 nm thick ALD deposited Al_2O_3 spacer layers. Low pressure of etching chamber and low RF power are the two crucial processing parameters for an ultrafine etching process with minimum damage and high aspect ratio of etched structures.[60–62] In a conventional RIE, RF power is predetermined in the ionization process such that the energy of bombarding radical is not independently controllable. By contrast, ICP-RIE is equipped with a RF source power to ionize precursor gas and another RF chuck power (called RF platen power) to control the energy of bombarding radicals. Following the complete etching of top spacer layer, the crosslinked PS pattern remaining between vertical Al_2O_3 spacers was removed by O_2 RIE and thermal calcination.

Figure 2 contrasts Al_2O_3 spacer layer coated lamellar PS nanopatterns and finally obtained pattern density doubled Al_2O_3 nanopatterns. 5-nm-thick Al_2O_3 films were conformal deposited at the surface of PS nanotemplate, as shown in Figures 2A and 2B. Highly aligned PS-*b*-PMMA vertical lamellae were spontaneously assembled within 1 μm wide photoresist trenches based on graphoepitaxy principle. The symmetric PS-*b*-PMMA used for Figure 2A had the M_n of 48 kg mol^{-1} for PS block and 46 kg mol^{-1} for PMMA block, respectively. The corresponding lamellar period (L_0) was 46 nm. By contrast, the M_n of PS-*b*-PMMA for Figure 2B was 25 kg mol^{-1} for PS block and 25 kg mol^{-1} for PMMA block, respectively, with the equilibrium L_0 of 28 nm. The thermal annealing was performed at 280 °C under inert N_2 atmosphere. The self-assembled film was irradiated with an UV lamp (λ = 255 nm), which selectively degraded PMMA domains while crosslinked the PS domains. After UV irradiation, the PMMA component was selectively removed by O_2 RIE (O_2 flow rate: 40 sccm, RIE power: 100 W & RIE chamber pressure: 60 mTorr). The 5-nm-thick Al_2O_3 spacer layers were deposited by ALD at the surface of remaining nanopatterned PS templates in a conformal manner.

Figures 2C and 2D show the Al_2O_3 nanopatterns, whose the pattern densities have been doubled from original BCP nanopatterns. For an effective removal of top Al_2O_3 spacer layer several etching conditions for ICP-RIE were tested. The optimal condition was found at the gas flow rate of Ar (20 sccm)/Cl_2 (10 sccm), RF source power of 1000 W, RF chuck power of 100 W and the chamber pressure of 10 mTorr. Subsequent RIE etching of PS was performed at the O_2 flow rate of 40 sccm, RIE power of 100 W and chamber pressure of 60 mTorr. In Figure 2C, the period of Al_2O_3 lamellar patterns were shrunken into 23 nm from 46 nm (Figure 2A), whereas in Figure 2D the period of Al_2O_3 lamellar patterns were shrunken into 14 nm from 28 nm (Figure 2B). The Al_2O_3 line width was given by original spacer layer thickness of 5 nm.

We also demonstrate ALD-assisted hole pattern shrinkage in **Figure 3**. Hexagonal arranged vertical cylinders were assembled

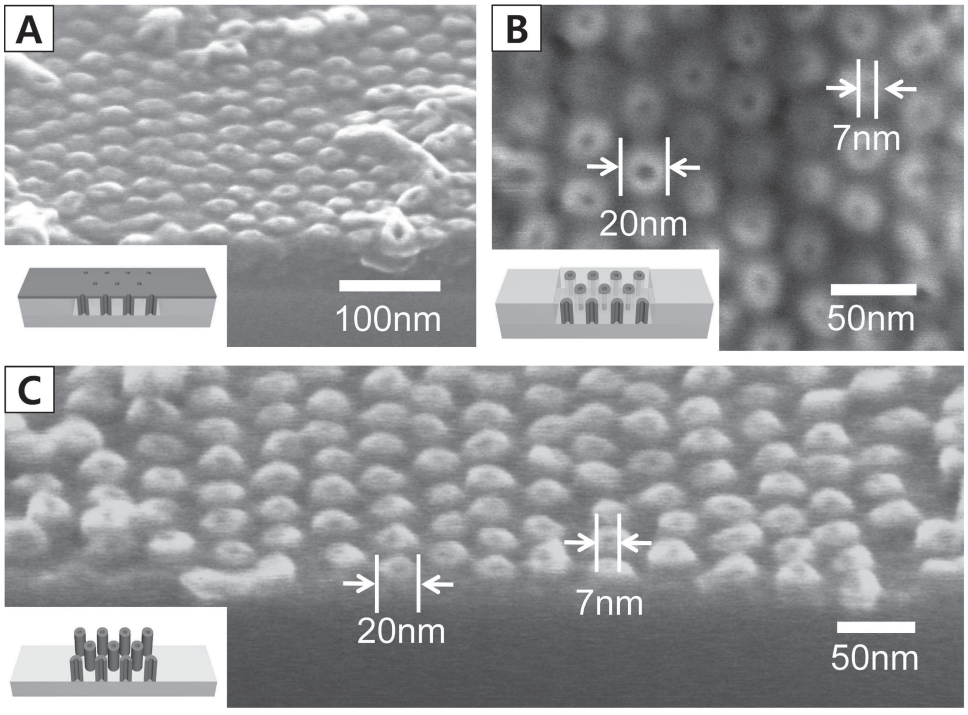

Figure 3. SEM images of hole pattern shrinkage with asymmetric PS-*b*-PMMA and ALD process. a) Al_2O_3 film deposited on PS-*b*-PMMA (M_n = 87 kg mol^{-1}) with the pattern period of 40 nm, b) hexagonally packed Al_2O_3 nanotubes with inner and outer diameters of 7 and 20 nm, respecively. Top Al_2O_3 layer was removed by ICP-RIE. c) Tilted images of Al_2O_3 nanotubes after RIE of PS polymers.

in a BCP film confined within 1 μm wide photoresist trench. The asymmetric PS-*b*-PMMA copolymer used for Figure 3 has M_n of 46 kg mol^{-1} for PS block and 21 kg mol^{-1} for PMMA block, respectively, whose cylinder layer period (L_0) is 40 nm. The BCP films were briefly treated with UV radiation and washed in acetic acid to selectively remove PMMA cylinder nanodomains. This wet etching minimizes the undesired etching of PS matrix and maintains the high aspect ratio of original BCP pattern. Figure 3A shows the nanoporous PS template coated with 5-nm-thick Al_2O_3 layer. ICP-RIE etching of the top spacer layer revealed the hexagonal packed Al_2O_3 nanotubes with 7 nm inner and 20 nm outer diameters (Figure 3B). The remaining PS template was thermally calcined at 380 °C under an ambient atmosphere. In Figure 3C, the resultant Al_2O_3 nanotubes with ≈30 nm heights are observed by tilted cross-sectional SEM. This precise nanotube patterning can be used for contact hole lithography for semiconductor industry[47,48,62] or functional nanotube array fabrication.[38,56]

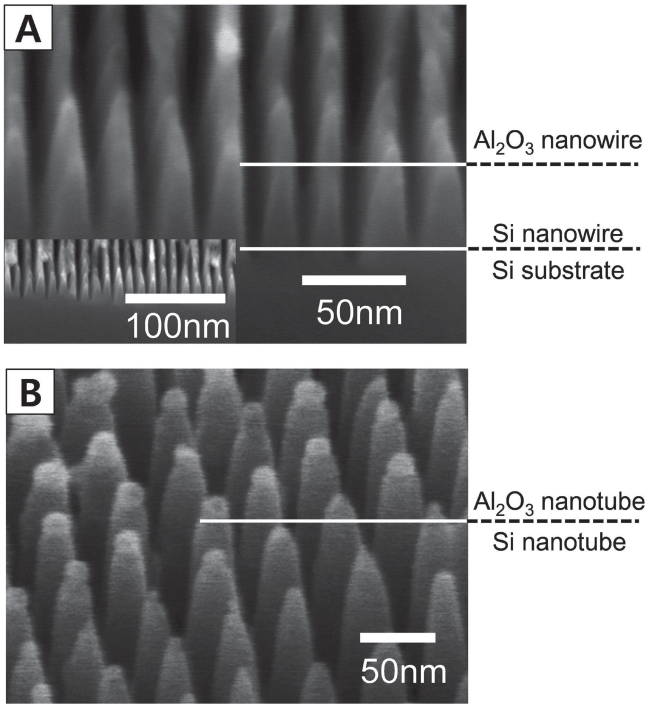

Figure 4. SEM images of ultrafine Si nanopatterns generated by ICP-RIE via nanopatterned Al_2O_3 etching masks. a) 5-nm-scale Si line arrays and b) Si nanotube arrays.

Owing to the high etch resistance, Al_2O_3 patterns can be further employed as a etching mask.[24,25,33,36] The ultrafine morphology of Al_2O_3 nanopatterns could be directly transferred into the underlying silicon substrate by ICP-RIE etching. In **Figure 4**A, the Si line pattern with 15 nm period and 5 nm line width have been successfully generated by ICP-RIE. The optimized ICP-RIE conditions were found at the gas flow rate of O_2 (8 sccm)/C_4F_8 (40 sccm), RF source power of 3000 W, RF chuck power of 75 W and ICP-RIE chamber pressure of 10 mTorr. The highly aligned nanoscale Si line arrays can be used as channel array elements for field effect transistors[16] or NAND flash memory devices.[40,44–49,62] In Figure 4B, the Si nanotubes were prepared by a similar pattern transfer process. Such a Si nanotube patterning can be directly used for the contact hole fabrication for semiconductor devices or field emitters for display applications.

3. Conclusion

We have demonstrated 5-nm-scale nanopatterning relying on BCP self-assembly successfully integrated with ALD assisted pattern multiplication. Significantly, our approach overcomes the intrinsic thermodynamic limitations of low χ BCPs for 5-nm scale downscaling. The self-limiting film growth and low temperature processing of ALD enable the direct conformal deposition of 5-nm thick Al_2O_3 spacer layer at organic BCP pattern surface without morphology distortion. Subsequent precise ICP-RIE accomplishes the pattern density multiplication for the minimum feature size of 5 nm. Notably, such ultrafine nanopatterns are achieved via single photolithographic exposing step employing conventional I-line lithography for 1 μm scale patterning (Overall, 200-fold enhancement of pattern density). Taken together, this novel approach offers 5-nm-scale nanopatterning with the minimum cost for lithographic tools. Besides, this ultrafine pattern multiplication method exploiting ALD is potentially integrated with other nanoscale lithography, including EUV lithography, nanoimprint and scanning probe lithography.[12,63,64]

4. Experimental Section

Substrate Preparation: A silicon substrate was cleaned by immersion in piranha solution (7:3 mixture of H_2SO_4 and H_2O_2) for 1 h at 110 °C and rinsed with deionized water. The cleaned substrate surface was neutrally modified by the covalent functionalization with P(S-*r*-MMA) copolymer brush layer. End-functional P(S-*r*-MMA) was spin casted from an organic solution and thermally reacted to the substrate surface at 160 °C for 24 h in a vacuum. Unreacted polymers were thoroughly spin washed with toluene.

Photoresist Confinement Preparation: A 100 nm thick photoresist layer (SU8, MicroChem Corp. US) was spin cast onto a silicon substrate and soft baked at 95 °C for 60 s to evaporate residual solvent and densify the film. The photoresist film was exposed to an I-line source (Midas/MDA-6000 DUV, KR; wavelength: 365 nm; 9.5 mW cm^{-2}) through a photomask and post baked at 110 °C for 95 s to selectively crosslink the exposed portions of photoresist film. The pattern development was performed by immersing the exposed photoresist film into propylene glycol methyl ether acetate (PGMEA) solution for 60 s.

Directed Self-Assembly of PS-b-PMMA Thin Films: For lamellar patterns, thin films of a symmetric PS-*b*-PMMA diblock copolymer having the number average molecular weights (M_n) of 48 kg mol^{-1} & 46 kg mol^{-1} or 25 kg mol^{-1} & 25 kg mol^{-1} for PS & PMMA blocks, respectively, were spin casted from a toluene solution over the photopatterned surface. Thermal annealing was conducted at 280 °C an inert N_2 atmosphere for the directed self-assembly into equilibrium morphology. In contrast, thin films of an asymmetric PS-*b*-PMMA diblock copolymer having the number average molecular weights (M_n) of 46 kg mol^{-1} & 21 kg mol^{-1} for PS & PMMA blocks, respectively, were spin casted from a toluene solution over the photopatterned surface, for cylinder patterns. Thermal annealing was conducted at 200 °C in a vacuum chamber.

ALD Deposition of TiO_2, ZnO and Al_2O_3 Thin Films: TiO_2, ZnO and Al_2O_3 thin films were deposited by Atomic Layer Deposition (ALD, iSAC/iOV E100). Titanium isopropoxide (TTIP), diethylzinc (DEZ) and trimethylaluminum (TMA) were used as Ti, Zn, and Al precursors. We note that after PMMA lamellae or cylinder nanodomains etching, the remaining UV or plasma treated PS nanotemplates revealed conformal deposition of ALD precursors over their entire surfaces, which contrast with sequential infiltration synthesis used for nanopore selective deposition. The unit cycle for metal oxide film included a metal precursor vapor pulse with 50 sccm of N_2 carrier gas, a purge pulse with 50 sccm of N_2, a H_2O vapor pulse with 50 sccm of N_2 carrier gas, and another 50 sccm N_2 purge pulse. The growth temperature on metal oxide ALD films has been conformed at temperatures ranging from 130 to 250 °C. The time period for one complete Al_2O_3 ALD cycle ranged from 20.4 s at 150 °C to 30.4 s at 130 °C, and the timing for TMA/purge/H_2O/purge sequence was 0.2/10/0.2/10 s at 150 °C and 0.2/15/0.2/15 s at 130 °C, respectively, The partial pressure for TMA during precursor exposure was ≈10 mTorr.

Etching of Al_2O_3 Thin Films: The Al_2O_3 spacer was etched by inductively coupled plasma reactive ion etching (ICP-RIE, Oxford Instruments/Plasmalab System 100). Optimized conditions were Ar (20 sccm)/Cl_2 (10 sccm), RF source power 1000W, RF chuck power 100 W and ICP-RIE chamber pressure 10 mTorr.

Pattern Transfer on Si Substrate: The Si substrate was etched by ICP-RIE. Optimized conditions were O_2 (20 sccm)/C_4F_8 (40 sccm), RF source power 3000W, RF chuck power 75 W and ICP-RIE chamber pressure 10 mTorr.

Charaterization: The nanoscale morphology of block copolymer thin film was imaged using a Hitachi S-4800 SEM with a field emission source at 1 kV.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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